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**Article Information** 

1. High-density chain ferroelectric random access memory (chain FRAM)

Takashima, D.; Kunishima, I.

Solid-State Circuits, IEEE Journal of

Volume: 33 Issue: 5 May 1998

Page(s): 787-792

Digital Object Identifier 10.1109/4.668994

Summary: A new chain ferroelectric random access memory-a chain FRAM-has been proposed. A memory cell consists of parallel connection of one transistor and one ferroelectric capacitor, and one

memory cell block consists of plural memory cells connected in ser.....

AbstractPlus | References | Full Text: PDF | IEEE JNL

2. Gain cell block architecture for gigabit-scale chain ferroelectric RAM

Takashima, D.; Oowaki, Y.; Kunishima, I.

VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on

1999

Page(s): 103-104

Digital Object Identifier 10.1109/VLSIC.1999.797251

Summary: Summary form only given. A ferroelectric RAM (FRAM), especially a chain FRAM, has great potential for future high-density nonvolatile memory. However, two severe problems inherent to

ferroelectric material make it difficult to realize gigabit scale F.....

AbstractPlus | Full Text: PDF | IEEE CNF

3. A sub-40-ns chain FRAM architecture with 7-ns cell-plate-line drive

Takashima, D.; Shuto, S.; Kunishima, I.; Takenaka, H.; Oowaki, Y.; Tanaka, S.

Solid-State Circuits, IEEE Journal of

Volume: 34 Issue: 11 Nov 1999

Page(s): 1557-1563

Digital Object Identifier 10.1109/4.799863

Summary: A nonvolatile chain FRAM adopting a new cell-plate-line drive technique was demonstrated.

Two key circuit techniques, a two-way metal cell-plate line and a cell-plate line shared with 16 cells,

reduce cell-plate-line delay to 7 ns and reduce plate dr.....

AbstractPlus | References | Full Text: PDF | IEEE JNL

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1. High-density chain ferroelectric random-access memory (CFRAM)

Takashima, D.; Kunishima, I.; Noguchi, M.; Takagi, S.

VLSI Circuits, 1997. Digest of Technical Papers., 1997 Symposium on

12-14 Jun 1997 Page(s): 83-84

Summary: Not available.....

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